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EXAMINER	
KROFCHECK, MICHAEL C	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,480	ADL-TABATABAI ET AL.	
	Examiner	Art Unit	
	Michael Krofcheck	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11, 13-21, 23-27, 29-33, 35-38, 40-47* is/are rejected.

7)☒ Claim(s) *12,22,28,34 and 39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/8/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/676,480 filed on 9/30/2003.

2. Claims 1-47 have been submitted for examination.

3. Claims 1-47 have been examined.

Specification

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

5. The abstract of the disclosure is objected to because the phrase, "a computer system is disclosed," is used in the first line. Correction is required. See MPEP § 608.01(b).

Claim Objections

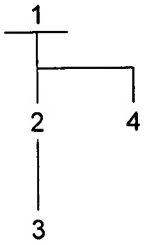
6. A series of singular dependent claims is permissible in which a dependent claim refers to a preceding claim which, in turn, refers to another preceding claim. A claim

which depends from a dependent claim should not be separated by any claim which does not also depend from said dependent claim. It should be kept in mind that a dependent claim may refer to any preceding independent claim. In general, applicant's sequence will not be changed. See MPEP § 608.01(n).

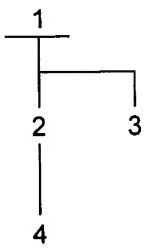
7. Claims 3-22, 29, and 43-47 are objected to because of the following informalities:

a. With respect to claims 3-22, and 43-47, the claims are improperly numbered. When viewing the claims in a claim tree, the claims should be numbered down their dependencies before being numbered across to claims on the same dependency level.

Claims should be numbered as:



Not as:



b. With respect to claims 43 – 47, it appears that the applicant intended to have these claims dependent on claim 42 not claim 1 as is written. The examiner will proceed under this assumption. The applicant is required to correct the appropriate claim dependencies.

c. With respect to claims 8 and 9, the term "are" should be inserted before the term "used."

d. With respect to claims 28 and 29, the multiple instances of the term "ore" should be changed to "or."

Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 3, 7-9, 13, 29, 44, 45 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claims 3, 44, and 45 recites the limitation "the cache controller" in line 1 of each respective claim. There is insufficient antecedent basis for this limitation in the claim.

11. Claim 7 recites the limitation "the companion lines" in line 1. There is insufficient antecedent basis for this limitation in the claim.

12. Claims 8 and 9 recites the limitation "the companion encoding bits" in line 1. There is insufficient antecedent basis for this limitation in the claim.

13. Claims 13 and 29 recites the limitation "the one or more companion bits" in line 2. There is insufficient antecedent basis for this limitation in the claim.

14. Claim 45 recites the limitation "the chipset" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

16. Claims 1-7, 9-11, 14, 17-18, 21, 23-27, 32-33, 35-37, and 41-47 are rejected under 35 U.S.C. 102(e) as being anticipated by Naffziger et al., U.S. Patent Application Publication 2003/0135694 (hereinafter Naffziger).

17. With respect to claim 1, Naffziger teaches of a computer system comprising: a central processing unit (CPU) (fig. 1, item 103; paragraph 0040); and

a cache memory, coupled to the CPU (fig. 1, items 104 and 106; paragraph 0040), having a plurality of compressible cache lines to store additional data (fig. 2; paragraphs 0043-0044; where the cache is organized into cache lines made up of multiple sublines which decompress to full cache lines).

18. With respect to claim 23, Naffziger teaches of a cache controller comprising: compression logic to compress lines within a cache memory device (figs. 2, 3; items 230, 308; paragraph 0051; where the compression engine compresses cache lines and sublines that contain partially uncompressed data into sublines); and

set and way logic to select cache lines (figs. 2-4; paragraph 0056-0059; where the tag address (set) is used to find a corresponding tag line and the way indicator

indicates where a cache line associated with the address tag is stored. Since the memory is addressable via address tags (sets) and ways, it is inherent that there is logic that selects the cache lines by this format).

19. With respect to claim 35, Naffziger teaches of a method comprising: determining if a first cache line within a cache memory device is to be compressed (fig. 3; paragraphs 0060; where if a cache line group (cache line comprising sublines) is compressible, the compression engine compresses it); and

compressing the first cache line (fig. 3; paragraphs 0060; where the compression engine compresses a cache line group if it is compressible).

20. With respect to claim 42, Naffziger teaches of a computer system comprising: a central processing unit (CPU) (fig. 1, item 103; paragraph 0040);

a cache memory, coupled to the CPU (fig. 1, items 104 and 106; paragraph 0040), having a plurality of compressible cache lines to store additional data (fig. 2; paragraph 0043-0044; where the cache is organized into cache lines made up of multiple sublines which decompress to full cache lines);

a chipset coupled to the CPU (fig. 1, items 103 and 110; paragraph 0040; the system controller and the processor integrated circuit makeup a chipset); and

a main memory (fig. 1, item 110; paragraph 0040).

21. With respect to claims 2 and 43, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein the computer system further comprises a cache controller to perform lookup operations of the cache memory (figs. 2, 3; items 240 and 330; paragraph 0062; The cache controller comprises

the cache control, compression & decompression engines, and all other components that work together to control the 2nd level cache memory (items 210 and 310). The cache control has writeback, read-ahead, and eviction control logic).

22. With respect to claims 3 and 44, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein the cache controller is included within the CPU (figs. 2, 3; paragraph 0041; where the cache controller is included in the second level cache, which is located on the processor integrated circuit).

23. With respect to claims 4, 24, and 46, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein the cache controller comprises an array of tags corresponding to each of the plurality of cache lines (fig. 3, 4; paragraph 0057-0059; where the address tag indicates where in the cache line group is the cache line associated with the address tag),

each tag having one or more compression encoding bits indicating whether a corresponding cache line is compressed (fig. 3, 4; paragraph 0057-0059, 0061; the address tag is associated with a compressed flag. The compressed flag indicates if the cache line is compressed).

24. With respect to claims 5, 25, and 47, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein a single cache line stores two or more cache lines if the corresponding compression bit indicates that the line is compressed (fig. 4-3; paragraphs 0043, 0059-0060 and 0066; where the cache line group (single cache line) stores multiple compressed cache lines, i.e. sublines.

When stored in compressed form, the remaining space in the group is usable by other groups associated with the excess address tags).

25. With respect to claim 6 and 26, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein each tag includes one or more companion encoding bits indicating which companion lines are stored in a common cache set (figs. 3-4; paragraphs 0059; where the way indicator (companion encoding bits) associated with each address tag indicates where in the cache line group (cache set) the cache line associated with the address tag is stored).

26. With respect to claim 7, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein the companion lines are adjacent memory lines (figs. 3-4; paragraphs 0059; where the data lines (companion lines) associated with the way indicators 0-15 are adjacent to each other).

27. With respect to claim 9, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein the companion encoding bits used to encode the ordering of companion lines in the compressed line (figs. 3-4; paragraphs 0059-0060; where the way indicator (companion encoding bits) associated with each address tag indicates where in the cache line group (cache line) the cache line associated with the address tag is stored. The cache line group is compressed in the cache data memory).

28. With respect to claim 10, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein the cache controller further comprises set and way selection logic to select a cache line (figs. 2-4; paragraph

0056-0059; where the tag address (set) is used to find a corresponding tag line and the way indicator indicates where a cache line associated with the address tag is stored. Since the memory is addressable via address tags (sets) and ways, it is inherent that there is logic that selects the cache lines by this format).

29. With respect to claims 11 and 27, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein the set and way selection logic comprises tag comparison logic to compare a cache line address to tags in the arrays of tags (figs. 2, 3; items 206, 320; paragraphs 0042 and 0062; where the tag comparator and hit logic compares the address field with the address tags).

30. With respect to claim 14, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein the cache controller further comprises compression logic to compress a cache line (figs. 2, 3; items 230, 308; paragraph 0051; where the compression engine compresses cache lines).

31. With respect to claim 17, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein the compression logic determines when a cache line is to be compressed (fig. 3, paragraph 0060; where the compression engine determines if a cache line group is compressible and compresses it if it is).

32. With respect to claim 18, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein the compression logic compresses a cache line based upon opportunistic compression (fig. 3; paragraph

0060; where the compression engine compresses the cache line group (cache line of compressed sublines) if it contains uncompressed data and is compressible).

33. With respect to claims 21 and 33, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein the cache controller further comprises byte selection logic to select addressed datum within a cache line (fig. 2; paragraph 0044; a first data line pointer from the tag memory is used to locate the first subline, the first subline is located within the cache line of compressed sublines, of the referenced information in the cache data memory. As the pointer is used to locate this subline, there must be logic that connects the pointer to the desired location).

34. With respect to claim 32, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein the compression logic determines when a cache line is to be compressed (fig. 3, paragraph 0060; where the compression engine determines if a cache line group is compressible and compresses it if it is).

35. With respect to claim 36, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein compressing the first cache line comprises storing data from a second cache line within the first cache line (fig. 4-3; paragraphs 0059-0060 and 0066; where the cache line group stores multiple cache lines with multiple sublines. When the cache line group is stored in compressed form, the remaining space in the group is usable by other groups associated with the excess address tags).

36. With respect to claim 37, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of analyzing a tag associated with the first cache line in a tag array to determine if the first cache line is compressed (fig. 3-4; paragraphs 0060-0061; where the decompression engine decompresses the data if the compressed flag (grouped with the address tag) indicates the data was compressed).

37. With respect to claim 41, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of using the one or more companion encoding bits to encode the ordering of companion lines in the first cache line if the first cache line is compressed (figs. 3-4; paragraphs 0059-0060; where the way indicator (companion encoding bits) associated with each address tag indicates where (the order) in the cache line group (cache line) the cache line associated with the address tag is stored. The cache line group is compressed in the cache data memory).

38. With respect to claim 45, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein the cache controller is included within the chipset (figs. 1-3; paragraph 0040-0041; where the cache controller is included in the second level cache, which is located on the processor integrated circuit, part of the chipset).

Claim Rejections - 35 USC § 103

39. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

40. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

41. Claims 15-16, 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naffziger.

42. With respect to claims 15 and 16, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of using various compression algorithms to compress cache lines (fig. 3; paragraph 0064). Naffziger fails to explicitly teach of using a dictionary based or sign-bit compression algorithm.

The applicant states in paragraph 48, "In one embodiment, cache lines are compressed according to a Lempel-Ziv compression algorithm. However in other embodiments, other compression algorithms (e.g., WK, X-Match, sign-bit compression, run-length compression, etc.) may be used to compress cache lines."

It would have been obvious to one of ordinary skill in the art to use a dictionary based or a sign-bit compression algorithm to compress cache lines. One would have been motivated to use a dictionary based compression algorithm as they are commonly

used in computers (such as the .gif and .zip formats), thus it would be compatible with numerous systems. One would have been motivated to use a sign-bit compression to compress cache lines as it would help to reduce the energy used to operate the cache memory.

43. With respect to claims 18-20, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of using various compression algorithms to compress cache lines (fig. 3; paragraph 0064). Naffziger fails to explicitly teach of using opportunistic, prefetch, or victim compression.

44. With respect to claims 30-31, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of using various compression algorithms to compress cache lines (fig. 3; paragraph 0064). Naffziger fails to explicitly teach of using a dictionary based or sign-bit compression algorithm.

The applicant states in paragraph 48, "In one embodiment, cache lines are compressed according to a Lempel-Ziv compression algorithm. However in other embodiments, other compression algorithms (e.g., WK, X-Match, sign-bit compression, run-length compression, etc.) may be used to compress cache lines."

It would have been obvious to one of ordinary skill in the art to use a dictionary based or a sign-bit compression algorithm to compress cache lines. One would have been motivated to use a dictionary based compression algorithm as they are commonly used in computers (such as the .gif and .zip formats), thus it would be compatible with numerous systems. One would have been motivated to use a sign-bit compression to

compress cache lines as it would help to reduce the energy used to operate the cache memory.

37. Claims 8 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naffziger and Yanai et al., U.S. Patent 5,206,939 (hereinafter Yanai).

38. With respect to claim 8, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger fails to specifically teach of wherein the companion encoding bits used as a compression format bit to select between different compression algorithms. However, Yanai teaches of compression format bits to select between different compression algorithms (table 3; column 7, lines 55-57; where bits 0-3 indicate the compression algorithm).

Naffziger and Yanai are analogous arts as they both are related to data compression. It would have been obvious to one of ordinary skill in the art having the teachings of Naffziger and Yanai at the time of the invention to incorporate the compression algorithm selection bits from Yanai into the way indicator in Naffziger in order to allow the different compression algorithms indicated in Naffziger to be indicated based on the way bits thus saving space in the cache memory and increasing the speed at which the data can be retrieved and decompressed.

39. With respect to claim 40, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger fails to specifically teach of using the one or more companion encoding bits as a compression format bit to select between different compression algorithms if the first cache line is compressed. However, Yanai teaches of using compression format bits to select between different compression algorithms if

the data is compressed (table 3; column 7, lines 55-57; where bits 0-3 indicate the compression algorithm).

Naffziger and Yanai are analogous arts as they both are related to data compression. It would have been obvious to one of ordinary skill in the art having the teachings of Naffziger and Yanai at the time of the invention to incorporate the compression algorithm selection bits from Yanai into the way indicator in Naffziger in order to allow the different compression algorithms indicated in Naffziger to be indicated based on the way bits thus saving space in the cache memory and increasing the speed at which the data can be retrieved and decompressed.

40. Claims 13 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naffziger and Gross, U.S. Patent Application Publication 2004/0255209 (hereinafter Gross).

41. With respect to claim 13, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger teaches of comparing a high order address field with address tags (paragraph 0062), but fails to specifically teach of wherein the tag comparison logic compares the one or more companion bits within the address with the one or more companion encoding bits within the tag if the compression encoding bits indicate that the cache line is not compressed.

However, Gross teaches of tag comparison logic compares the one or more companion bits within the address with the one or more companion encoding bits within the tag if the compression encoding bits indicate that the cache line is not compressed (fig. 2; paragraph 0021, where the high address part (companion bits) is compared by

comparators (comparison logic) against the way addresses (companion encoding bits) to determine if the address has stored a hit in the cache. Cache hits are determined if a cache line is compressed or uncompressed. Therefore, they occur when the cache line is uncompressed).

Naffziger and Gross are analogous arts as they are both in the same field of endeavor, data compression in a cache memory. It would have been obvious to one of ordinary skill in the art having the teachings of Naffziger and Gross at the time of the invention to include the logic that compares the high address part in with the way addresses located in the tag address in Gross into the tag compare logic in Naffziger. The motivation for this would have been to more accurately determine cache hits by comparing more of the addresses.

42. With respect to claim 38, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger teaches of comparing a high order address field with address tags (paragraph 0062), but fails to specifically teach of analyzing one or more companion encoding bits if the first cache line is not compressed.

However, Gross teaches of analyzing one or more companion encoding bits if the first cache line is not compressed (fig. 2; paragraph 0021, where the high address part is compared against the way addresses (companion encoding bits) to determine if the address has stored a hit in the cache. Cache hits are determined if a cache line is compressed or uncompressed. Therefore, they occur when the cache line is uncompressed).

Naffziger and Gross are analogous arts as they are both in the same field of endeavor, data compression in a cache memory. It would have been obvious to one of ordinary skill in the art having the teachings of Naffziger and Gross at the time of the invention to compare the high address part in Naffziger with the way addresses located in the tag address in Naffziger as is done in Gross. The motivation for this would have been to more accurately determine cache hits by comparing more of the addresses.

43. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Naffziger and Wang et al., U.S. Patent 6,507,895 (hereinafter Wang).

44. With respect to claim 19, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger teaches of compression logic (figs. 2-3, items 230 and 308), but fails to specifically teach of compresses a cache line based upon prefetch compression

However, Wang teaches of compresses a cache line based upon prefetch compression (column 6, lines 14 – 20; where prefetch data can be compressed and stored in a compression cache).

Naffziger and Wang are analogous arts as they both involve data compression in a cache. It would have been obvious to one of ordinary skill in the art having the teachings of Naffziger and Wang at the time of the invention to modify the compression engine and control logic in Naffziger to compress prefetched data as is done in Wang. The motivation for this would have been to provide faster access (Wang, column 6, lines 14 – 20).

45. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Naffziger and Shimoi et al., U.S. Patent 5,652,857 (hereinafter Shimoi).

46. With respect to claim 20, Naffziger teaches of all the limitations of the parent claims as discussed supra. Naffziger teaches of compression logic (figs. 2-3, items 230 and 308), but fails to specifically teach of compresses a cache line based upon victim compression.

However, Shimoi teaches of compresses a cache line based upon victim compression (fig. 7, column 10, line 61-column 11, line 12; where the uncompressed data in the cache memory is swept out buy the LRU and the compressing circuit compressed the data and stores it in the compression cache memory).

Naffziger and Shimoi are analogous arts as they both involve data compression in a cache. It would have been obvious to one of ordinary skill in the art having the teachings of Naffziger and Shimoi at the time of the invention to modify the compression engine and control logic in Naffziger to compress data evicted from the L1 cache and store it in the L2 cache as taught in Shimoi. The motivation for this would have been to improve the capacity while limiting the costs of the system, Shimoi column 1, lines 21 - 23.

Allowable Subject Matter

45. Claims 12, 22, 28, 34, and 39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

46. Claim 29 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

47. The following is a statement of reasons for the indication of allowable subject matter:

a. With respect to claims 12, 28, and 39, the prior art fails to teach of wherein the tag comparison logic ***ignores*** the one or more companion encoding bits within the address if the one or more compression encoding bits indicate that the cache line is compressed.

b. With respect to claims 22 and 34, the prior art of Naffziger teaches of a decompressor. The prior art of Alvarez, II et al Patent Application Publication 2001/0054131 teaches of a multiplexer to select between a decompressed cache line and a compressed cache line (fig. 8; paragraph 0203). The prior art fails to specifically teach of an output multiplexer to select between companion lines in the uncompressed cache line as is taught in the claims.

Double Patenting

38. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir.

1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

39. Claim 1 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/676,478. Although the conflicting claims are not identical, they are not patentably distinct from each other see chart below.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Application 10/676,480	Application 10/676,478	Application 10/747,470	Application 10/747,474
Claim 1: A computer system comprising: a central processing unit (CPU); and	Claim 1: A computer system comprising: a central processing unit (CPU); and	Claim 1: A computer system comprising: a central processing unit (CPU);	Claim 1: A computer system comprising: a central processing unit (CPU);
a cache memory, coupled to the CPU	a cache memory, coupled to the CPU,	a cache memory, coupled to the CPU,	a cache memory, coupled to the CPU,
having a plurality of compressible cache lines to store additional data.	including: a main cache having a plurality of cache lines that are compressible to store additional data; and	having a plurality of compressible cache lines to store additional data;	having a plurality of compressible cache lines to store additional data;
	a plurality of storage pools to hold a segment of the additional data for one or more of the plurality of cache lines that are to be compressed.		
		and a cache controller, coupled to the cache memory, to reorder a cache line after each access to the cache line prior to the compression of the cache line into a compressed cache line.	

			and a cache controller, coupled to the cache memory, including: compression logic to compress one or more of the plurality of cache lines into compressed cache lines; and hint logic to store hint information in unused space within the compressed cache lines.

Conclusion

40. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

41. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

42. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

43. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael Krofcheck

MATTHEW D. ANDERSON
PRIMARY EXAMINER